

TITLE 400G QSFP-DD OPEN ZR+ 120km DCO High TX Power	DOC No. RFD-20231023003-001	
	REVISION : 01	AUTHORIZED BY : Andy Yang
	DATE : 2023.10.24	CLASSIFICATION : CONFIDENTIAL

1.Introduction

This document describes the product specifications for 400G OpenZR+ QSFP-DD DCO modules based on DP-16QAM supporting extended C-band, polarization diversity coherent detection and advanced electronic link equalization. Chromatic dispersion compensation can be applied to the receive side of the demodulator. This module is managed utilizing the Two Wire Interface that is specified in the Common Management Interface Specification (CMIS). The module has following system performance and features:

1. Support Flex-grid channel spacing DWDM in C-band
2. Support Client-side Interfaces: 1*400GAUI-8/4*100GAUI-2 for 400G OpenZR+
3. Support Line-side: DP-16QAM with CFEC(ZR), DP-16QAM with oFEC(OpenZR+)
4. High TX Power up to +3dBm
5. Integrated TOF is optional
6. 76pin QSFP-DD MSA compliant connector
7. Compliant to CMIS 5.0
8. Compliant to OIF Implementation Agreement for Coherent CMIS, Rev 01.1 9. OIF-400ZR-02.0
10. OIF OpenZRplus_2p0
11. RoHS compliant

1.1 Typical Application

The application field of the module is widely used from short haul (ZR) to Metro(MR) interconnects. As shown in figure1, it is comprised of high-data lanes, a single 3.3V power supply, an IIC interface for module control and status report, and dedicated alarm and control pins (not shown on the figure1).

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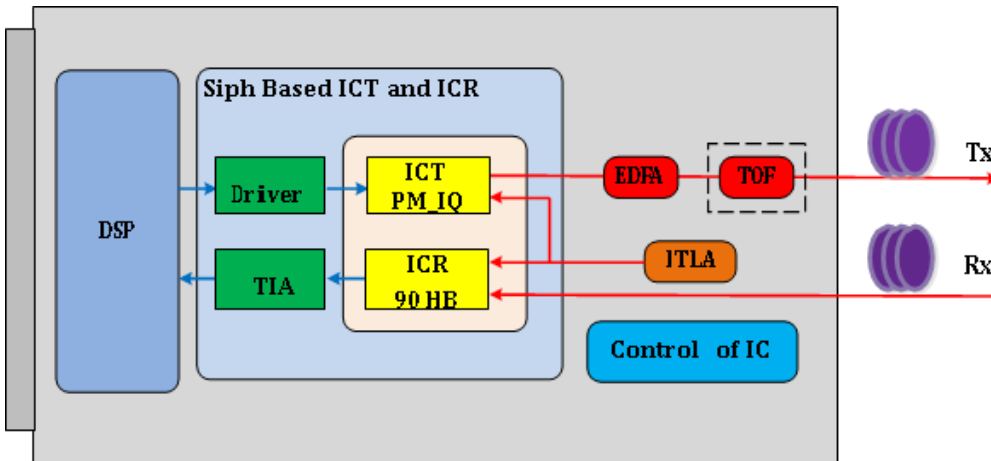


Figure 1: Functional Diagram of Module

1.2 Module Description

The module uses a 76-pin QSFP-DD MSA QSFP-DD Hardware Specification connector for all electrical interfaces with the host card, whereas the optical interfaces on the line side are provided through the optical receptacles on the QSFP-DD. The module can be partitioned into three functional parts: TX path, RX path and Control & Power block.

1.3 Path Description

The host interface is comprised of a total of 8 high-speed SerDes lanes. This allows module to support two interfaces for 400G application: an independent double 4-Lane mode client interfaces (for 1*400GbE application) and four independent double lane mode client interfaces (for 4*100GbE application).

2.PRODUCT DESCRIPTION

2.1PRODUCT NAME AND SERIES NUMBER(S)

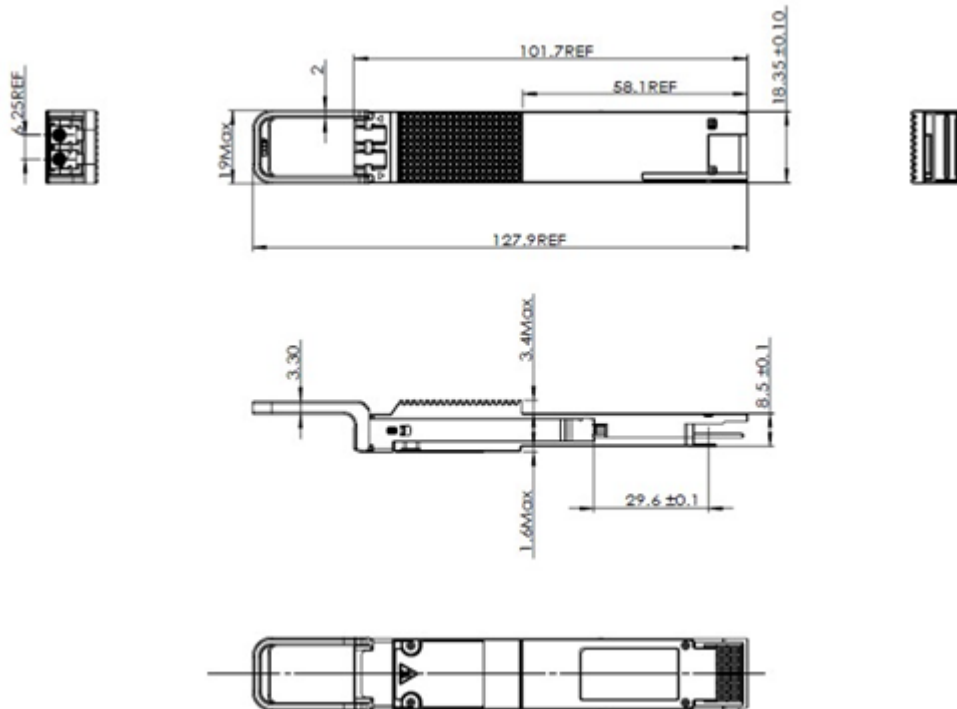
400G QSFP-DD OPEN ZR+ DCO

Part Number	Data Rate	POWER(dBm)	SEN(dBm)	Temp	Modulation
P6637ZGQCVT2-1	400G	-5~3	-20	C	PAM4

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2.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING

The pluggable module fully compliant with the QSFP-DD Type 2 Module Specification, including dimensions and tolerances for the connector, cage and module system. The module shall be designed to be inserted into a host board with a railing system that includes a heat sink.



3. Product Specification

3.1 Absolute Maximum Ratings

Id	Parameter	Min	Max	Unit	Note
1	Storage Temperature	-40	85	°C	
2	Storage Humidity (Relative)	-	85	%	no-Condensing
3	Case Temperature	0	75	°C	

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4	Operating Humidity (Relative)	-	85	%	no-Condensing
5	Short term Operating Case Temperature		80	°C	<24 hours
6	Power Supply Absolute Range	-0.3	3.63	V	
7	RX Optical Maximum Input Power	-	10	dBm	

3.2 Recommended Operating Conditions

Id	Parameter	Min	Max	Unit	Note
1	Operating Case Temperature	0	70	°C	
2	Operating Humidity (Relative)	-	85	%	no-Condensing
3	Power Supply Operating Range	3.135	3.465	V	
4	RX Optical Input Power	-	0	dBm	

3.3 Power Supply

Id	Parameter	Min	Typ.	Max	Unit	Note
1	3.3V DC Power Supply Voltage	3.135	3.3	3.465	V	
2	3.3V DC Power Supply Current			8	A	
3	Power Dissipation (400G OpenZR+)			21.5	W	
4	Low Power Consumption			1.5	W	
5	Module Inrush Current			100	mA/us	
6	Turn-off Current	-100			mA/us	

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7	Power Supply Noise			25	mV	
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3.4 Transceiver Electrical Characteristics

Id	Parameter	Min	Typ.	Max	Unit	Note
1	Signal Rate, each Lane	26.5625±100ppm			GBaud	
2	Differential Peak-Peak Input Voltage Tolerance			900	mVpp	

3.5 Receiver Electrical Characteristics

Id	Parameter	Min	Typ.	Max	Unit	Note
1	Signal Rate, each Lane	26.5625±100ppm			GBaud	
2	Differential Peak-Peak Input Voltage Tolerance		750	900	mVpp	
3	Transition Time, 20% to 80%		9.5		ps	

3.6. Optical Characteristics of Transmitter

Id	Parameter	Min	Typ.	Max	Unit	Notes
1	Transmitter requery Range	191.3	193.7	196.1	THz	C band 75GHz ITU-T grid. Frequency range over which the specifications hold unless noted otherwise.
2	Laser Frequency Stability	-1.8		1.8	GHz	Frequency stability relative to ITU grid.
3	Laser Frequency Accuracy	-1.8		1.8	GHz	
4	Laser Frequency Fine Tuning Range	-6.0		6.0	GHz	

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5	Fine Tuning Resolution		100		MHz	
6	Channel Tuning Speed	-		60	s	
7	Laser LineWidth			100	kHz	
8	Transmitter Output Power Range	-5		3	dBm	
9	Transmitter Laser Disable Time			180	ms	
10	Output Power Stability	-0.5		0.5	dB	Difference over temperature, time, wavelength and aging.
11	Output Power Accuracy	-2		2	dB	Difference between the set value and actual value over aging.
12	Transmitter Turn-up Time from Cold Start	-		120	s	
13	Transmitter OSNR (Inband)	34		-	dB/0.1nm	
14	Transmitter OSNR (Our of band)	TBD			dB/0.1nm	Spec for CTFQDS400SZPTA00, TOF version
15	Transmitter Back Reflectance	-		-24	dB	
16	Transmitter Output Power with TX Disabled	-		-20	dBm	
17	Transmitter Polarization Dependent Power	-		1.5	dB	Power deference between X and Y polarization

3.7. Optical Characteristics of Receiver

Id	Parameter	Min	Typ.	Max	Unit	Notes
1	Receiver Frequency Range	191.3	193.7	196.1	THz	
2	Input Power Range	-12		0	dBm	Signal power of the channel at the OSNR Penalty < 0.5dB
3	OSNR Sensitivity		22	24	dB/0.1nm	

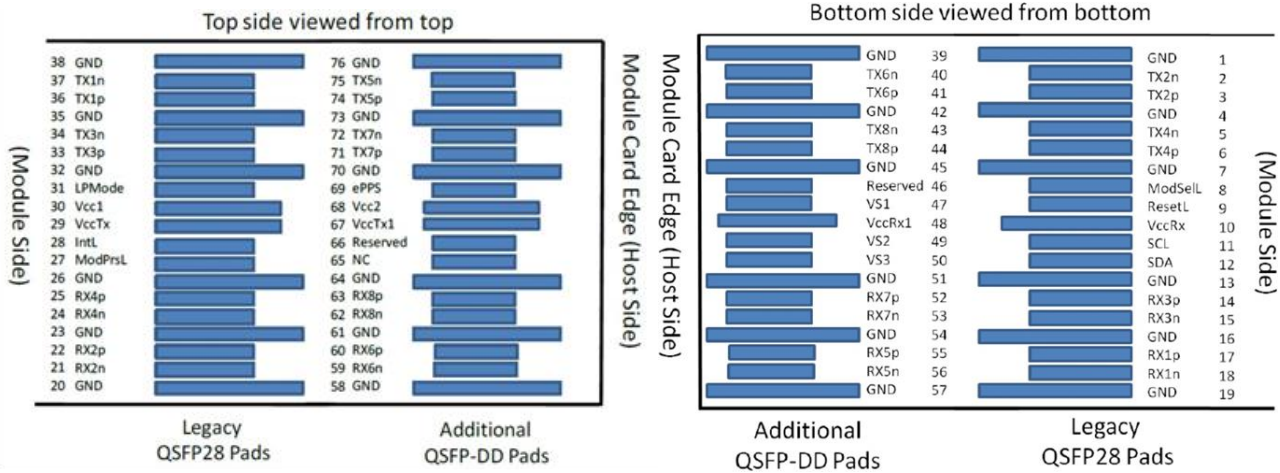
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4	Receiver Sensitivity			-20	dBm	Input power needed to achieve post FEC BER < 1E-15 when OSNR Tolerance > 26dB/0.1nm
5	CD Tolerance	9000			ps/nm	Tolerance to CD with 0.5 dB penalty to OSNR sensitivity when change in SOP is 1 rad/ms.
6	PMD Tolerance	20			ps	Tolerance to PMD with < 0.5 dB penalty to OSNR sensitivity.
7	Peak PDL Tolerance	3.5			dB	Tolerance to peak PDL with < 1.3 dB penalty to OSNR sensitivity when change in SOP is < =1 rad/ms.
8	Tolerance to Change in SOP	50		-	rad/ms	
9	Input Power Transient Tolerance	-2		2	dB	Tolerance to change in input power with <0.5 dB penalty to OSNR sensitivity.
10	Input Power Reading Accuracy	-2		2	dB	
11	Optical Return Loss	20			dB	Optical reflectance at Rx connector input.
12	Receiver Turn-up Time from Cold Start	-		120	s	From module reset, with valid optical input signal present.

4.Host Electrical Connector & Pin Assignments

The electrical interfaces, including pad assignments for data, control, status and power supplies and host PCB layout requirements, of the module is fully compliant with the QSFP-DD MSA QSFP-DD-Hardware Specification, Rev 5.0. The case of the QSFP-DD module is isolated from the module's circuit ground, GND, to provide the equipment designer flexibility regarding connections between external electromagnetic interference shields and circuit ground, GND, of the module.

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Pad Function Definition

Pin #	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	

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17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTTL-O	ModPrsL	Module Present	3B
28	LVTTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A

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43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For Future Use	3A
70		GND	Ground	1A

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71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

5.Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2023/10/24	Andy Yang	Mike Sun